NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA



[An Institute of National Importance under Ministry of Education, Govt. of India]
Sector 1, Rourkela, Sundergarh Dist., Odisha 769 008

SPONSORED RESEARCH INDUSTRIAL CONSULTANCY CONTINUING EDUCATION

NITR / SR / 2025 / Advt.- 25EC005 / L / 035

dt.18-Jun-2025 Ref: FTS 250617-8806

SR-R03

Advertisement for Recruitment of Project Position

Candidates who fulfill the below mentioned criteria may submit the application form before the last date. Engagement will be purely on temporary / contractual basis and co-terminus with the completion of the project. Candidates are advised to go through the advertisement details carefully before applying.

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|--|---|---------------------------------------|--|---|--|
| 1. | Title of the Project: | Design and Developm | ent of Deep Learning based Secure Jo | int Channel Estimation and Feedback. | |
| 2. | Project Code, Dept. with Closing Date: SR/25/EC/005 16-Dec-2027 Electronics and Communication Engg. | | | | |
| 3. | . Funding Agency Details: Department of Telecommunication (DOT) - | | | | |
| 4. | PI details: | Prof. Shrishailayya | M Hiremath | hiremaths @nitrkl.ac.in, 0661-246 2459 | |
| | | 9438503621 | - | hiremaths @ gmail.com | |
| 5. | Co-PI details: | Prof. R P Naik, P S | ingh, B Palit and S Behera | setshri @nitrkl.ac.in, 0661-246 4691 | |
| | | - | - | - @ gmail.com | |
| 6. | 6. Details of the Post(s): | | 7. Educational Qualification & Working Knowledge | | |
| Res | earch Fello | ow (RF) | Essential Qualification (s): | | |
| | [Name of the Post(s)] | | B.Tech/B.E/B.Sc(Engg) (with valid GATE/NET score) in ECE, EE, EC, EEE, EI, Telecommunication, Applied Electronics, Communication and Networks, CSE or related specializations pertaining to Telecommunication, signal processing, wireless and RF communication and VLSI and Embedded system, Information technology, AI and MI, with minimum 60% marks or 6.5/10 CGPA for throughout the carrier. | | |
| 01 | (One) | 03 Year(s), 00 Month(s) | M.Tech/M.E/M.Tech(R)/MS in Electronics and Communication, Telecommun | nication, Applied Electronics, Communication and Networks, Signal Lon, RF Communication, VLSI and Embedded system, AI and ML , Computer | |
| | [No. of Post(s)] (Tenure of Post) | | or | | |
| Yea | ır 1 & 2 | | M.SC/MCA(with valid GATE/ NET/ Any national fellowship) in Electronics and Communication, Telecommunication, Applied Electronics, Communication and Networks, Signal processing Communication and Signal processing, Wireless Communication, FC Communication, VLSI and | | |
| | VR 42.000 | .00 /- per month | Embedded system, AI and ML , Computer networks, CSE, any allied specialization, with minimum 60% marks or 6.5/10 CGPA for both postgraduate and undergraduate courses. | | |
| | 111 3000 | | | | |
| (+ | | | Experience / Software / Skillset & Desirable (| Qualification: | |
| |) HRA @ N | A % (if applicable) | Experience / Software / Skillset & Desirable (| · | |
| Year |) HRA @ N | A % (if applicable) | 1.The candidate should have a basic understanding of Signal F Probability, and Linear Algebra / Optimization / Machine Lear | Processing, Digital Communication, MIMO Communication, rning algorithms. 2. Strong programming skills in languages such | |
| Year |) HRA @ N · 3 NR 42,00 0 | A % (if applicable) .00 /- per month | 1.The candidate should have a basic understanding of Signal F Probability, and Linear Algebra / Optimization / Machine Lear as C, C++, Python, MATLAB, VHDL, or Verilog are essential, al communication models. 3. Exposure to hardware platforms such | Processing, Digital Communication, MIMO Communication, rning algorithms. 2. Strong programming skills in languages such long with experience in deep learning frameworks and wireless as SDR, FPGA, or RF-SOC is desirable. 4.Familiarity with EDA | |
| Year |) HRA @ N · 3 NR 42,00 0 | A % (if applicable) | 1.The candidate should have a basic understanding of Signal F Probability, and Linear Algebra / Optimization / Machine Lear as C, C++, Python, MATLAB, VHDL, or Verilog are essential, al communication models. 3. Exposure to hardware platforms such | Processing, Digital Communication, MIMO Communication, rning algorithms. 2. Strong programming skills in languages such long with experience in deep learning frameworks and wireless as SDR, FPGA, or RF-5oC is desirable. 4.Familiarity with EDA ate or postgraduate candidates in the above specializations are institute's regulations. Candidates without a valid GATE | |

Carry out research in the specified area of the project, including the following tasks: collecting CSI datasets, designing algorithms for joint channel estimation and feedback, developing deep learning techniques, implementing adversarial attacks and corresponding mitigation strategies, and developing joint sensing solutions on SDR/RF-SoC platforms.

Online Interview details: 07-Jul-2025 10:00 AM Department of Electronics and Communication Engg.

Application link for eligible candidate(s): NIT Rourkela Homepage ⇒ FACULTY & STAFF ⇒ SRICCE ⇒ Career ⇒ Notices

The candidate(s) are required to send the complete filled and signed application (soft copy) with documents regarding educational qualification indicating percentage of marks / division (mark-sheets and / or certificates), research papers (if any), work experience certificate (if any) etc., This may be built as a single PDF file and sent by email with "Advertisement No." on the subject link to the above mentioned e-mail IDs. NO hard copies of application(s) are required to be sent to the Institute.

Last date for submitting the Application: 04-Jul-2025

The period of experience in a discipline / area of work, wherever prescribed, shall be counted after the date of acquiring the minimum prescribed educational qualifications for that position. Mere possession of minimum qualification does not guarantee invitation to the interview. Candidates will be short listed based on merit and need of the project. Selection / Joining will be cancelled in case of any suppression of information / document submitted.

NIT Rourkela reserves the right to fix higher criteria for short-listing of eligible candidates from those satisfying advertised qualification and requirement of the project post. Only short-listed candidates will be informed for Online interview. In case, any clarification is required on eligibility regarding the above post, the candidate may contact in the above mentioned details.

Age Guideline: The upper age limit for applying for the award of project position shall be 32 years, which is relaxed up to 5 years in the case of candidates belonging to Schedule Castes / Schedule Tribes / PWD and Female applicants whereas 3 years in the case of OBCs (Non-creamy layer candidates). Upper age limit shall be reckoned as on the last date of receipt of applications.

Any other terms & conditions governed as per guidelines issued by the funding agency for the engagement of above position as amended from time to time shall be in force towards this temporary recruitment.

Sd/-Asst. / Dy. / Jt. Registrar (SR)

Copy to:

- > PI & CO- PI: Prof. Shrishailayya M Hiremath , EC & Prof. R P Naik, P Singh, B Palit and S Behera EC > Chairman, DRC, Dept. of EC
- > Head of the Department / Centres / Units (It is requested that the contents of the above advertisement be brought to the notice of the staff(s) / student(s) working in your Deptt. / Centre / Unit.)
- Dealing Seat (SR Project Recruitment)
 Advertisement File

→ To publish advertisement at NITR website.