NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA

[An Institute of National Importance under Ministry of Education, Govt. of India]
Sector 1, Rourkela, Sundergarh Dist., Odisha 769 008
SPONSORED RESEARCH INDUSTRIAL CONSULTANCY CONTINUING EDUCATION

NITR / SR / 2025 / Advt.- 25EC020 / L / 058 dt. 06-Aug-2025 **Ref: FTS** 250805-4336 **SR-R03**

Advertisement for Recruitment of Project Position

Candidates who fulfill the below mentioned criteria may submit the application form before the last date. Engagement will be purely on temporary / contractual basis and co-terminus with the completion of the project. Candidates are advised to go through the advertisement details carefully before applying.

1.	Title of the Project:	Designing On-Chip Memory for Space Internet of Things: Safeguarding Against Attacks and Radiation.		
2.	Project Code, Dept. with Closing Date:	SR/25/EC/020	-NA-	Electronics and Communication Engg.
3.	Funding Agency Details:	ISRO-STIC Rourkela		-
4.	PI details:	Prof. Arjun Singh Yadav	yadavas@nitrkl.ac.in, 0661-246 2482	
		9713871191	-	- @ -NA-
5.	Co-PI details:	Prof. Kunal Singh	-@nitrkl.ac.in, 0661-246 -	
		7985201453	-	kunalsingh.ece@nitjsr.ac.in @ -NA-

6. Details of the Post(s):

Junior Research Fellow (JRF)
[Name of the Post(s)]

01 (One) *[No. of Post(s)]*

03 Year(s), 00 Month(s) *(Tenure of Post)*

Year 1 & 2
INR 37,000.00 /- per month
(+) HRA @ NA % (if applicable)

Year 3
INR 42,000.00 /- per month
(+) HRA @ NA % (if applicable)

7. Educational Qualification & Working Knowledge

Essential Qualification (s):

1. Master's degree (M.Tech. in Electronics & Communication/ VLSI/ Microelectronics or similar equivalent specialization) with ≥6.5 CGPA or 60% marks with valid GATE score.
2. M.Sc. (with GATE/NET/GPAT) in Electronics or similar with 65% marks or 7.0/10 CGPA.
3. Bachelor's degree holders (B.Tech in Electronics and Communication/ Electrical and Electronics/ Electrical/ Electronics/ Instrumentation/ Computer Science and Engineering or similar equivalent branch of engineering) with ≥7.0 CGPA or 65% marks and valid GATE.

Desirable Qualification:

1. Preferred with Valid GATE Score
2. Knowledge of Digital VLSI, Analog VLSI, Physical VLSI Design, and CAD Tool of VLSI Design
3. Experience of handling VLSI CAD Tool.

Job Description:

To conduct research in physical VLSI design using the CAD tool such as Cadence Design Environment, focusing on memory design with a capacity of 2 MBytes, including IC tapeout, packaging, and testing. Additionally, JRF will have to visit ISRO for project follow-up. Opportunity to enroll as a Ph.D. scholar in the Department of Electronics and Communication Engineering, NIT Rourkela.

Notified Later	Interview details:	-	- -	Department of Electronics and Communication Engg.

Application link for eligible candidate(s): NIT Rourkela Homepage ➡ FACULTY & STAFF ➡ SRICCE ➡ Career ➡ Notices

The candidate(s) are required to send the complete filled and signed application (soft copy) with documents regarding educational qualification indicating percentage of marks / division (mark-sheets and / or certificates), research papers (if any), work experience certificate (if any) etc., This may be built as a single PDF file and sent by email with "Advertisement No." on the subject link to the above mentioned e-mail IDs. NO hard copies of application(s) are required to be sent to the Institute. Last date for submitting the Application: **10-Sep-2025**

The period of experience in a discipline / area of work, wherever prescribed, shall be counted after the date of acquiring the minimum prescribed educational qualifications for that position. Mere possession of minimum qualification does not guarantee invitation to the interview. Candidates will be short listed based on merit and need of the project. Selection / Joining will be cancelled in case of any suppression of information / document submitted.

NIT Rourkela reserves the right to fix higher criteria for short-listing of eligible candidates from those satisfying advertised qualification and requirement of the project post. Only short-listed candidates will be informed for Online interview. In case, any clarification is required on eligibility regarding the above post, the candidate may contact in the above mentioned details.

Age Guideline: The upper age limit for applying for the award of project position shall be 28 years, which is relaxed up to 5 years in the case of candidates belonging to Schedule Castes / Schedule Tribes / PWD and Female applicants whereas 3 years in the case of OBCs (Non-creamy layer candidates). Upper age limit shall be reckoned as on the last date of receipt of applications.

Any other terms & conditions governed as per guidelines issued by the funding agency for the engagement of above position as amended from time to time shall be in force towards this temporary recruitment.

-NA-

Sd/-
Asst. / Dy. / Jt. Registrar (SR)

Copy to:

- PI & CO- PI: Prof. Arjun Singh Yadav , EC & Prof. Kunal Singh EC
- Chairman, DRC, Dept. of EC
- Head of the Department / Centres / Units (It is requested that the contents of the above advertisement be brought to the notice of the staff(s) / student(s) working in your Deptt. / Centre / Unit.)
- Dealing Seat (SR – Project Recruitment)
- Advertisement File
- → *To publish advertisement at NITR website.*