



**NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA – 769 008(ODISHA)  
SPONSORED RESEARCH, INDUSTRIAL CONSULTANCY & CONTINUING EDUCATION**

**NITR/SR/2022/Advt-22EE083/L/004, dt.08.04.2022.**

Applications are invited on prescribed format for the following assignment in a purely time bound research project undertaken in the Department of Electrical Engineering of the Institute.

1. Name of the Temporary Post : **JRF - 01 ( Project Code: SR/22/EE/083).**
2. Name of the Research Project : **Vertical integration to Fabricate 2T and 4T GaAs/Si Tandem PV device (TOPCON)**
3. Name of the Sponsoring Agency : SERB, New Delhi
4. Tenure of the Project : 03 Years (Mar 2022- Mar 25)
5. Tenure of the Assignment : Up to 03 Years or End of the project
6. Job Description : Research project implementation and documentation and whatever needed to execute the project successfully
7. Consolidated monthly compensation / Fellowship : Rs. 31,000/- pm (for first 2 years)  
Rs. 35,000/- pm (till project end-date)
8. Essential Qualifications and experience : M.Tech./ME/M.S. in Electrical/ Electronics/ Communications/ Instrumentation or equivalent or Microelectronics/Solid state Technology/MEMS/Nano Science/Nano Technology/Material Science/Engineering Physics or equivalent, relevant to the area of research  
OR  
B.Tech./BE in Electrical/Electronics/Communications / Instrumentation or equivalent or Microelectronics/Solid state Technology/MEMS/Nano Science/Nano Technology/Material Science/Engineering Physics or equivalent, and having a CGPA/CPI score of 8.00 (out of 10.0)  
and above with valid GATE score can apply
9. Desirable Qualifications/ Experiences : Master's degree with experience of prior research work, journal publication/s, knowledge in – semiconductor fabrication and characterization, - is highly desirable. Candidates with research experience as JRF or equivalent will be given preference. Candidate is expected to join immediately.
10. Accommodation : Bachelor accommodation in the Institute may be provided subject to availability.

(P.T.O)

11. For technical information on the project, the candidate may contact the Principal Investigator at the following address:

Name : Dr. Paresh Govind Kale  
Address : 431, Department of Electrical Engineering  
N.I.T., Rourkela-769 008  
Telephone No : 0661-2462447 (O)  
E-mail : [pareshkale@nitrkl.ac.in](mailto:pareshkale@nitrkl.ac.in) or [paresh.iitb@gmail.com](mailto:paresh.iitb@gmail.com)

Date and Time for **On-line Interview: 20.04.2022 at 09.00 AM**

Eligible candidates may apply within **18.04.2022, 2359 HRS**. The candidates are required to send the complete filled up application form (Soft copy) to [pareshkale@nitrkl.ac.in](mailto:pareshkale@nitrkl.ac.in)

The application form is available in the following link:  
[http://nitrkl.ac.in/oldwebsite/Jobs\\_Tenders/5ProjectFellowships/Doc/JRF%20LS-PND-64\(2\).pdf](http://nitrkl.ac.in/oldwebsite/Jobs_Tenders/5ProjectFellowships/Doc/JRF%20LS-PND-64(2).pdf)which must be filled by candidates and also required to attach photocopies of all supporting documents, research papers (if any)etc.

Candidates will build a Single PDF file; it is to be sent to Principal Investigator ([pareshkale@nitrkl.ac.in](mailto:pareshkale@nitrkl.ac.in)) **on or before 18.04.2022, 2359 HRS**. The candidates are also required to produce relevant documents mentioned in the application form [such as original of all mark sheets and certificates, research papers (if any), experience certificate (if any) etc.] at the time of interview / joining. Selection / Joining will be canceled in case of any suppression of information / document provided earlier.

Mere possession of minimum qualification does not guarantee invitation to the interview. Candidates will be short listed based on merit and need of the project.

Sd/-  
Asst. Registrar (SRICCE)

Copy to : 1) All Heads of the Departments, NIT, Rourkela for publication on Departmental Notice Boards.  
2) Dr. Paresh Kale (EE), co-Principal Investigator with a request to give wide publicity to advertisement.  
3) Head of the Department, EE  
4) Project file.