Summer Course
on
Analog and Digital VLSI Design

(30th June – 12th July 2025)

Patron:

Prof. K. Umamaheshwar Rao,
Director, NIT Rourkela

Chairman:

Prof. K. K. Mahapatra,
Professor HAG, Dept. of ECE

Coordinators:

Dr. Sougata Kumar Kar
Dr. Sudip Kundu
Dr. Arjun Singh Yadav

Department of Electronics and Communication Engineering,
National Institute of Technology Rourkela
Rourkela-769008, Odisha, India

Technically Co-sponsored by:

IEEE ROURKELA SUBSECTION

About Institute: **NIT Rourkela** is one of the premier national level institutions for technical education in the country and is funded by the Government of India. Government of India has elevated the Regional Engineering College, Rourkela to a deemed university under the name of National Institute of Technology, Rourkela.

Please visit https://www.nitrkl.ac.in/

Rankings - 2024

34 NIRF Overall	19 NIRF Engg.	30 NIRF Research

About Department: The department of **Electronics and Communication Engineering** was established with the vision to become a nationally acclaimed department of higher learning that will serve as a source of knowledge and expertise for the society. The department offers various UG and PG programmes with the mission to advance and spread knowledge in the areas of Electronics, Communication, Instrumentation, Signal processing, Microwave and Radar and VLSI leading to creation of wealth and welfare of humanity. The department also offers Ph. D. for regular as well as sponsored candidates. The faculties of EC department are handling several externally funded research projects. Please visit

https://www.nitrkl.ac.in/EC/

Relevance of Summer Course:

India has identified semiconductors as a strategic sector, launching initiatives like the ₹76,000 crore Semiconductor Mission and the PLI Scheme to boost chip manufacturing and design. However, there is a shortage of skilled manpower in this domain. Therefore, there is a growing need for engineers with hands-on experience in VLSI and embedded systems. In this context, the summer course is particularly relevant.

Today both ASIC (analog and digital) and FPGA are essential in building complex systems. While ASICs offer high performance and low power consumption, FPGAs provide flexibility and rapid prototyping capabilities. Understanding both design paradigms equips engineers to respond effectively to evolving industry demands.

This course offers practical exposure to industry-standard tools and methodologies for design of analog and digital ICs and FPGA development. Students will work with tools such as Cadence, VHDL/Verilog, synthesis platforms, and simulation environments, providing them with a competitive edge in the job market.

Course objectives:

1. **Introduction to CMOS technology** and its applications in analog and digital IC design.
2. **Design of CMOS analog building blocks.**
3. **Exploration of digital CMOS logic circuits.**
4. **Hands-on experience** with circuit simulation tools (e.g., **Cadence Virtuoso**, **FPGA**).
5. **Bridge the gap between theory and real-world design** through lab sessions.
6. **Prepare students for careers or research in VLSI design**, analog/digital IC development, and the semiconductor industry.

Important Dates:

Registration Deadline	**15th June 2025**
Fee Payment	**15th June 2025**

Topics to be covered (tentatively)

Analog IC Design

- ✓ MOS Fundamentals
- ✓ Single Stage amplifiers
- ✓ Current Mirrors
- ✓ Differential Amplifier
- ✓ Two Stage Operational Amplifier
- ✓ Current References
- ✓ Voltage References
- ✓ CMOS Comparator
- ✓ Analog to Digital Converters (ADC)
- ✓ Digital to Analog Converters (DAC)
- ✓ Analog Layout Design

Digital IC Design

- ✓ VLSI Design Flow, Verilog HDL
- ✓ RTL Best Practices, FSMs
- ✓ Linting: Concepts, Tools, Common RTL errors
- ✓ Synthesis: Timing Constraints, Reports
- ✓ Low Power VLSI Design Techniques
- ✓ Physical Design
- ✓ VLSI Testing
- ✓ ATPG, BIST, Scan Chains
- ✓ Introduction to FPGA
- ✓ FPGA Implementation

Hands-on lab sessions: 3 hrs/day (total 36 hrs); Tools: Cadence (Virtuoso, Xellium, Genus, Conformal, Innovus); Synopsys (VCS, Design Vision), Xilinx Vivado

Target Participants:

B. Tech. / B.E., M.E. / M. Tech / MS students, research scholars/professionals, faculty members working / planning to work in future in the area of Microelectronics and VLSI. Specialization: ECE, EI, EE, or related branches.

Speakers:

Prof. Kamalakanta Mahapatra
Prof. Debiprasad Priyabrata Acharya
Prof. Sougata Kumar Kar
Prof. Atin Mukherjee
Prof. Santanu Sarkar
Prof. Ayas Kanta Swain
Prof. Sumit Saha
Prof. Arjun Singh Yadav
Prof. Sudip Kundu

Selection criteria and intimation:

Limited seats (20) !!!
Selection will be based on
(1) Previous academic performance
(2) Statement of purpose (SOP)
(3) Specialization of previous/present degree
(4) First come first serve basis

Certificate:

Upon successfully completing the course.

Facilities:

No travel allowance will be provided.

Shared accommodation and food on payment basis (**INR 3000 approx. in hostel on sharing basis, to be paid during check-in**).

Registration:

For online registration, after fee payment, fill the google form: https://forms.gle/MuD6jBzDhUGgneAd9

Format for Self-declaration:

I, [Full Name], a [UG/PG/PhD] student/faculty of Dept. of [Name of the Department] from [Institution Name], want to attend the summer course titled "Analog and Digital VLSI Design", which is scheduled to take place from 30th June to 12th July 2025 at NIT Rourkela.

I hereby certify that the above information is correct.

Signature of the applicant
Date and place.

Registration fee:

- **INR 10000 + 18% GST (INR 11800) for students**
- **INR 15000 + 18% GST (INR 17700) for faculty members / professionals**

Merchant Name : CONTINUING EDUCATION NIT

Contact and Queries: Please send your queries directly to the course coordinators.

Coordinators:

Dr. S. K. Kar	kars@nitrkl.ac.in, 9692951945
Dr. S. Kundu	kundus@nitrkl.ac.in, 7070170510
Dr. A. S. Yadav	yadavas@nitrkl.ac.in, 9713871191