National Institute of Technology Rourkela

Departmental Seminar

Seminar Title	: Leakage-Attack-Resilient Modified 8T SRAM Cell with Enhanced Write Stability.
Speaker	: Neha Khute
Supervisor	: Prof Arjun Singh Yadav
Venue	: EC303, Seminar Room
Date and Time	: 29 Aug 2025 (2.00PM)
Abstract	: Power analysis attacks have become a major problem in VLSI circuits. The attackers extract sensitive information of SRAM cells through side-channel attacks (SCAs), and hence, leakage power analysis attack (LPAs) has become a serious concern to the security systems. To provide reliability and security to these cells, a modified leakage-attack-resilient 8T (MLAR-8T) SRAM cell has been proposed. The simulations are done using Cadence Virtuoso in 65nm CMOS technology at 27°C. The proposed single-cell SRAM MLAR-8T exhibits a 0.943x shorter write access time (WAT) than the existing LAR-8T @V_{DD} = 1V. Also, the proposed cell consumes 4.15x/ 1.90x lower dynamic power than 6T/ LAR-8T, respectively. However, these gains come at the expense of a larger read delay and lower read stability.