National Institute of Technology Rourkela

Departmental Seminar

Seminar Title	: Low Power ALU Design using Pre-Computational LUT for RV32M Processor.
Speaker	: Mirza Aman
Supervisor	: Prof S Sarkar
Venue	: EC303, Seminar Room
Date and Time	: 29 Aug 2025 (05.00PM)
Abstract	: This paper presents a Look Up Table(LUT) based pre-computational(PC) Arithmetic Logic Unit(ALU) for RV32M. The proposed ALU provides low power consumption and high speed for application specific purpose where the input of the ALU is repeated several times. The proposed ALU integrates LUT based on pre-computational mechanism with the multiplier and control logic unit which store the computational results of frequent operands. The system avoids unnecessary arithmetic operations, thereby reducing the real time computations allowing to increase speed and reduce dynamic power consumption. Simulation results shows substantial reduction in power consumption without compromising much in the operational speed proposed ALU design making it suitable for energy-constrained applications with frequent operands such as DSP and CNN based application. This pre-computation technique gives promising direction for enhancing energy efficiency in processor design.