National Institute of Technology Rourkela

Defence Seminar

Seminar Title	: Design and Performance Analysis of Soft-Error Hardened Storage Cells for Radiation-Prone Applications
Speaker	: Sandeep Kumar (Rollno : 519ec1008)
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Venue	: Offline: EC seminar hall (EC 303) Online: https://tinyurl.com/9ys9kca7 (MS Teams Link)
Date and Time	: 13 May 2025 (11:25 AM)
Abstract	: This work presents the design of soft-error (SE) hardened storage elements, including latches, flip-flops, and SRAM cells, targeting radiation-prone applications. Our designed SNUSH, DNUSH, DNUCR, and TNUSH latches are optimized for single (SNU), double (DNU), and triple node upsets (TNU). SNUSH latch offers a cost-effective SNU-resilient solution with low power, area, and delay. DNUSH and DNUCR latches achieve higher DNU robustness, with DNUCR latch exhibiting the lowest power, delay, and PDAP among state of the art works. TNUSH latch is designed for TNU resilience, outperforming existing designs in speed and PDAP. These latches were extended to master-slave flip-flops, offering improved SE robustness and efficiency. Additionally, we developed SE-hardened SRAM cells (SERSC-16T, HP-16T, and SEH-14T), capable of recovering from SNUs and DNUs under high charge injections, with superior stability, delay, and power metrics. These SRAM cells are capable of recovering from SNUs even after injecting a large amount of charge. Moreover, DNUs at internal node pairs of these SRAM cells show recoveries for a substantial amount of charge injection. A 128-byte SE-hardened synchronous SRAM block, built using the proposed designs, demonstrates their effectiveness in radiation prone environments.