National Institute of Technology Rourkela

Progress Seminar

Seminar Title	: Design and Analysis of Low Power Radiation-Hardened SRAM Cells for Aerospace Applications
Speaker	: Soumya Sengupta (Rollno : 521ec1008)
Supervisor	: Arjun Singh Yadav
Venue	: EC-303 Seminar Room
Date and Time	: 28 May 2025 (10:00 AM)
Abstract	: In conventional memory cells like SRAM, used in satellite and aerospace applications, exposure to high amounts of radiation causes single node upset (SNU) and dual node upset (DNU) that changes the storage state of the SRAM cell. This usually results in one bit flipping from &rdquo0&rdquo &rarr &rdquo1&rdquo and from &rdquo1&rdquo &rarr &rdquo0&rdquo, respectively. As technology scales down, the capacitance of the nodes of such cells has been drastically reduced, thereby creating nodes that are more vulnerable to SNU and DNU. Therefore, the rate of soft error generation that causes SNU and DNU is enhanced with technology scaling in the nanometre regime. Reduction or scaling of the supply voltage further makes the circuits more prone to radiation and decreases the critical charge. Therefore, a need arises for designing SNU and DNU-tolerant radiation-hardened SRAM cells to improve the resilience of SRAM designs against radiation effects. This work presents two novel RHBD SRAM cell designs, such as radiation-hardened SRAM cell (RHSC-14T) and radiation-tolerant (RT-20T) SRAM cell, that have the capability to recover from single node upsets (SNU) induced at sensitive nodes and dual node upsets (DNU) caused at sensitive storage node-pairs. RHSC-14T and RT-20T provide 100% SNU and DNU recoverability and have the least number of sensitive nodes and sensitive node pairs. The fault tolerance of RHSC-14T is enhanced by isolating the charge storage nodes (Q-QB) from internal nodes (S0-S1) using two NMOS transistors (N2 and N4) in the pull-up path that prevents the fault from propagating to the internal nodes of the circuit. The simulation was performed in Cadence Virtuoso in UMC 65nm CMOS technology at 27 ° C and @VDD = 1V. The layout of all the designs has also been performed in 65nm CMOS technology. The performance of the proposed RHSC-14T and RT-20T has been determined over NS10T, QUCCE12T, QCCS, SCCS, DNUCTM, DNUSRM, QCCM12T, S4P8N, S8P4N, SCCS18T, CC18T, and LPDNUR by comparing with design parameters such as read delay, write delay, Static Noise Margin (SNM), critical charge, hold power, relative area, radiation sensitive area, and radiation occurrence probability. A comparative analysis on design metrics such as delay and power has been performed with PVT (process corner-voltage-temperature) variation, and a 5000 Monte Carlo simulation has also been performed on HSNM, RSNM, and WSNM to determine the robustness of the proposed designs under worst-case corner. In addition to estimating the superiority of the proposed designs over existing state-of-the-art RHBD SRAM cells, the performance quality metric (PQM) has been considered, which takes into account all design metrics. However, these gains come at the expense of a larger area overhead.