National Institute of Technology Rourkela

Progress Seminar

Seminar Title	: Design of Low Power SAR ADC for Bio-Medical Applications
Speaker	: Deepika Kumaradasan (Rollno : 521ec1012)
Supervisor	: Prof. Santanu Sarkar
Venue	: EC Seminar Room, EC303
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Abstract	: For diagnosing and treating diseases in medicine and healthcare systems, the prerequisites of portable, energy-efficient, battery-operated electronic devices are rapidly boosting biomedical applications. An analog-to-digital converter (ADC) is a significant part of an implantable pacemaker that converts the analog input to digital output for storage and/or further processing for future utilization. An 8-bit 100 kS/s Low Power SAR ADC with modified EPC and supply voltage of 1.8 V is designed with a sinusoidal input signal of 390.625 Hz, which achieves an SFDR of 54.94 dB, an SNDR of 48.21 dB, and an ENOB of 7.71 bits, respectively. The proposed 8-bit SAR ADC devours a total power consumption of 0.05 mW. A modified EPC is proposed to improve the delay without much compromise in the power consumption, and it is observed that the delay of the modified EPC is reduced by 2.5 times the conventional EPC. An 8-bit SAR ADC with a dual-path bootstrapped switch and triple-tail comparator is designed with a supply of 1.8 V. The speed and linearity of the switch are improved by utilizing the primary signal path and the secondary signal path in the dual-path bootstrapped switch. The Triple Tail comparator provides low noise/offset and devours a low power consumption. The SAR ADC produces an SFDR of 60.42 dB, SNDR of 49.81 dB, and ENOB of 7.98 bits, respectively, for a 3.906 kHz signal frequency sampled at 1 MS/s based on the realization of the FFT spectrum. There is a static DNL error of 0.004 LSB and an INL error of 0.013 LSB, respectively, which consumes approximately 34.81 &muW of power in total. The proposed 8-bit SAR ADC with an enhanced EPC consumes power of about 40.5 &muW. It achieves a DNL of 0.004 LSB, an INL of 0.015 LSB, and dynamic performance characteristics with a simulated SNDR of 48.15 dB, an SFDR of 55.52 dB, and an ENoB of 7.7 bits, respectively, for a 50.781 kHz input signal at 1 MS/s sampling frequency. The 10-bit SAR ADC with LSB&rsquos C-MOSCAP DAC uses approximately 90.11 &muW of power, according to the simulation results. It attains an 813.802 Hz input signal at 833.33 kS/s sampling frequency, a DNL of 0.0025 LSB, an INL of 0.0049 LSB, and dynamic performance characteristics with a simulated SNDR of 59.69 dB, an SFDR of 70.57 dB, and an ENoB of 9.62 bits, respectively. The 8-bit SAR ADC with an enhanced EPC and a proposed randomized DEM 8x8 CDAC has a power consumption of 73.34 &muW. It achieves a DNL of 0.004 LSB, an INL of 0.018 LSB, and dynamic performance characteristics with a simulated SNDR of 49.53 dB, an SFDR of 62.96 dB, and an ENoB of 7.934 bits, respectively, for a 50.781 kHz input signal at 1 MS/s sampling frequency.