National Institute of Technology Rourkela

Registration Seminar

Seminar Title	: Performance Assessment of Vertical TFET for Signal Processing Applications
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Venue	: EE 401
Date and Time	: 29 Jan 2025 (17:15)
Abstract	: In VLSI/ULSI circuits, the Tunnel Field Effect Transistor (TFET) has come out as a very good alternative for low-power applications. To counteract short-channel effects like DIBL, velocity saturation, quantum confinement, and velocity degradation, TFETs can have a better alternative than compared with conventional MOSFETs. TFETs have a gated p-i-n profile and band-to-band tunneling (BTBT) mechanism. To have low power consumption, the Tunnel Field Effect Transistor (TFET) relies on decreasing the supply voltage with downscaling. MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) are useful for the low power application generally. The structure of MOSFET and TFET resembles each other with a different working mechanism. TFET has a gated p-i-n profile, and the current conduction takes place by band-to-band tunneling (BTBT) mechanism, through a barrier in between the energy bands of the channel and source. The design and optimization of a p-type Vertical Tunnel Field-Effect Transistor (VTFET) featuring a SiGe pocket for enhanced performance is investigated. The device structure comprises a vertical architecture with the drain at the top, a silicon channel, a SiGe pocket adjacent to the channel, and a heavily doped source at the bottom. The inclusion of the SiGe pocket, with a germanium content optimized at 40%, enhances band-to-band tunneling (BTBT) by reducing the tunneling barrier height, thereby improving the on-state current significantly. Key parameters such as the gate work function (5.4eV), source doping concentration, and channel dimensions (60 nm channel length with a 5 nm SiGe pocket) are tailored to optimize device behavior. The study demonstrates a marked improvement in ION, as well as a reduction in subthreshold swing (SS), making the device suitable for low-power and signal-processing applications. However, challenges such as ambipolar current at higher biases and threshold voltage VTH adjustment are addressed through strategic doping and SiGe composition tuning. Simulation results obtained using the Silvaco tool reveal the p-type VTFET's potential for high-performance, energy-efficient electronics, particularly in applications requiring ultra-low power and high switching speeds. This work highlights the advantages of incorporating SiGe pockets in vertical TFETs and provides a pathway for future research into advanced semiconductor devices.