National Institute of Technology Rourkela

Departmental Seminar

Seminar Title	: A Capacitance Mismatch Cancellation Technique for Differential Capacitive Interfacing Circuit.
Speaker	: Ipsita Dash.
Supervisor	: Prof Sougat Kar
Venue	: VLSI Lab
Date and Time	: 03 Jan 2025 (05.15PM)
Abstract	: A Capacitance Mismatch Cancellation Technique for Differential Capacitive Interfacing Circuit Authors: Ipsita Dash, R.Maheswari , Sougata Kumar Kar, Santanu Sarkar. Name of the conference: IEEE-INDICON 2024, IIT Kharagpur, Kharagpur, India. Abstract: This paper describes a mismatch cancellation technique for switched capacitor-based differential capacitance inter- facing circuits. The capacitive sensor can detect the small change in capacitance in the range of femto Farad which is converted into a differential voltage employing the interfacing circuit. Among the various sensors, capacitive sensors are adopted because of their improved sensitivity, better temperature performance and low power dissipation. The voltage-mode compensation for eliminating capacitance mismatch in MEMS accelerometers is introduced. The interface circuit comprises a buffer, comparator, counter, low pass filter, offset reduction strategy, and a fully differential operational amplifier. The proposed circuit can minimise errors caused by the circuit components, such as DC offset. The comparator compares the output voltage of the interfacing circuit with the common mode voltage to decide how much voltage is needed to compensate for charge imbalance, calibration voltage is generated with the help of a DAC (digital to analog converter). The introduced circuit has been designed and simulated using UMC 0.18-µm CMOS process technology. Keywords— Capacitive sensor system, Interfacing circuit, signal conditioning, Calibration voltage.