| Departmental Seminar | |
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| Seminar Title | : Navigating the Challenges of Dynamic Quantum Circuits for IoT Gateway. |
| Speaker | : Jaganath Prasad Mohanty |
| Supervisor | : Prof K K Mahaptra |
| Venue | : VLSI Lab |
| Date and Time | : 03 Jan 2025 (11.00AM) |
| Abstract | : This paper explores the potential of dynamic quantum circuits with fault tolerance in enhancing Internet of Things (IoT) gateways. By allowing real-time adaptability and incorporating robust error correction mechanisms, dynamic quantum circuits can significantly improve the security, efficiency, and reliability of IoT systems. The adaptability of these circuits enables them to respond to changing conditions and errors, making them well-suited for the complex and often unpredictable nature of IoT environments. However, the implementation of dynamic quantum circuits presents several challenges. These include the complexity of circuit design, the need to manage high error rates, increased resource requirements, and the integration of quantum systems with existing classical architectures. Additionally, developing effective real-time feedback mechanisms and ensuring robust security measures are critical for maintaining the integrity of these advanced systems. Despite these challenges, the potential benefits of dynamic quantum circuits in IoT applications are substantial. As research progresses and technology advances, overcoming these obstacles could lead to the realization of smarter, more resilient IoT environments that leverage the unique capabilities of quantum computing. This integration has the potential to drive innovation across various sectors, ultimately enhancing everyday life and transforming how we interact with technology. |