
Seminar Title	: Design of Low Power Front End for Multi-Channel EEG Signal Acquisition System
Speaker	: H Prem Sai Kumar (Rollno : 520ec1010)
Supervisor	: Dr. Sudip Kundu
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Abstract	: There is an exponential increase in brain disorder problems. To understand the underlying disease, the brain signal is captured. This technique is commonly known as the electroencephalogram (EEG). The signals are captured from different parts of the brain for better diagnosis. EEG signals are commonly acquired through multiple sensors placed on the brain. This makes the EEG system as multi-channel. The multi-channel EEG signal acquisition system consists of multiple single-channel signal acquisition units. A single-channel EEG signal acquisition unit comprises electrodes and an electronic circuit.

The EEG signal captured by the electrodes is very small in magnitude (of the order of a few hundred microvolts) and suffers from common mode noise. Therefore, the first block of the electronic circuit is the instrumentation amplifier (INA), which amplifies the captured signal and at the same time removes the common mode noises. It may be noted that the magnitude of the common mode noise is much higher than captured EEG signal. Therefore, INA should have a high common mode rejection ratio (CMRR). In addition to the high CMRR, the issues faced during the design of an INA are DC offset, flicker noise, etc. There are different types of INA architectures, such as three-opamp topology, current feedback instrumentation amplifier (CFIA) topology, and capacitively-coupled chopper instrumentation amplifier (CCIA) topology. Out of all these, CCIA is one of the most promising topologies because of its capability to remove $1/f$ noise, rail-to-rail sensing, high gain accuracy, and suitability for low-power design. The CCIA also removes the electrode offset (EOS) and internal DC offset of the amplifier. Therefore, the CCIA-based INA will be used in each channel to design the multi-channel EEG signal acquisition system. Apart from INA, a single-channel signal acquisition system includes a programmable gain amplifier (PGA) and analog-to-digital converter (ADC). All these blocks consume significant power and area. So, in the multi-channel signal acquisition system, these blocks will be shared to optimize power and area.

The CCIA's performance directly depends on the operational transconductance amplifier (OTA) performance. While designing the CCIA, an efficient OTA demarcated through high gain, high bandwidth, low noise, high common mode rejection ratio (CMRR), and low power is always desirable. In this work, a single-stage efficient high-gain adaptive recycling folded cascode (HGARFC) OTA is proposed.

The HGARFC OTA is used in the planned CCIA architecture. Further, the designed HGARFC OTA has been included in a two-channel TDM-based signal acquisition system, and its performance has been tested using two input signals. Apart from this, to optimize power and area in a signal acquisition system, a variable gain INA (VINA) is designed. In addition to this, to optimize power and area in CCIA, a Split-HGARFC (SHGARFC) OTA is designed. Further, the SHGARFC OTA is used in the proposed two-channel TDM-based signal acquisition system design.