NATIONAL INSTITUTE OF TECHNOLOGY
ROURKELA-769008 (ODISHA)
An Institute of National Importance under Ministry of Education, GOI

NOTICE INVITING TENDER

Tender Notification No: NITR/PW/EC/2021/258 Dated: 16/04/2021

The National Institute of Technology, Rourkela invites bids from the eligible bidders for procurement of **Standard ETT-101 BisKit Telecom's experimenter** at NIT Rourkela.

Last date of Submission of Bid **: 06/05/2021 by 03:00 PM**

Opening date of techno-commercial Bid **: 07/05/2021 at 03:00 PM**

For Details: http://nitrkl.ac.in/OldWebsite/Jobs_Tenders/9Equipment/Default.aspx

Contact: Prof. Poonam Singh
Department of Electronics & Communication Engineering,
NIT Rourkela, Odisha- 769008.
Email ID: psingh@nitrkl.ac.in

Bidding through: https://eprocure.gov.in/eprocure/app

Sd/-
REGISTRAR

NATIONAL INSTITUTE OF TECHNOLOGY
ROURKELA-769008, ODISHA

OPEN TENDER NOTICE NO.: NITR/PW/EC/2021/258 Dated: 16/04/2021

Procurement of Standard ETT-101 BisKit Telecom's experimenter

SL.NO	Description of Goods/Service	Quantity
1.	Standard ETT-101 BisKit Telecom's experimenter	10 units

1. Quantity required **: As mentioned above (All information regarding technical specification mentioned in Annexure II in Tender Documents)**
2. Delivery **:** Within **60 days** from the date of purchase order
3. **Last Date of submission of Bid : 06/05/2021 by 03:00 PM**
4. **Date of opening of techno-commercial bid : 07/05/2021 at 03:00 PM**
5. The firm should not have been black listed at any time.
6. The submission of following bids by the tenderer should be through https://eprocure.gov.in/eprocure/app. Please follow the guidelines as per the portal.

Procurement of Standard ETT-101 BisKit Telecom's experimenter

(Open Tender Notice No.: NITR/PW/EC/2021/258 Dated: 16/04/2021)

Due on 07/05/2021 by 03:00 PM

7. **Liquidated damage clause** will be charged for any delay in supply of goods.
8. The validity of the tender shall be **90 days** from the date of opening of the techno-commercial bids.
9. Detailed advertisement including all tender documents is also available in our website at http://nitrkl.ac.in/OldWebsite/Jobs_Tenders/9Equipment/Default.aspx .
10. NIT reserves the right to qualify or deny prequalification of any or all applicants without assigning any reasons.

(REGISTRAR)
NIT, Rourkela
Fax No- 0661-2462022
Ph. No -0661-2462021

ANNEXURE-II

DETAILED TECHNICAL SPECIFICATION

Specifications for Standard ETT-101 BisKit Telecom's experimenter:

Sealed tender bids are invited from reputed/authorized vendors/companies for Standard ETT-101 BisKit Telecom's experimenter with following tender specifications.

Sl. No.	Name of goods	Specifications
1.	Standard ETT-101 BisKit Telecom's experimenter	Each experimenter kit should consist of following modeling blocks: Adder (2 off), Multiplier (3 off), Twin Pulse Generator, Dual Analog Switch, Noise Generator, Buffer, Channel Module (band pass filter and low pass filter), Utilities (Comparator, Rectifier, Diode& RC LPF, RC LPF). Tuneable Low Pass filter, Variable DCV, Speech (microphone), EXOR (gate), VCO, Sequence Generator, Divider, PCM Encoder, Master Signals, Serial to Parallel, PCM Decoder and Expansion (connector}. Detailed specification of each modeling block is listed below. Detailed system specification (of each experimenter kit) is listed below. ETT-101 means Emona ETT-101 BisKit Telecom Experimenter. Picture of kit is attached below.

MODELING BLOCKS SPECIFICATIONS

Adder 1:

Dual input

Variable gain from 0 to 2 (inverting)

Bandwidth approx. 600kHz

Adder 2:

Dual input

Fixed gain of 1

Bandwidth approx. 600kHz

Amplifier:

Bandwidth DC to approx. 600kHz

gain 0.2 to 10

Channel Module:

CHANNEL BPF

F_{center} = 100kHz;

Passband = 24kHz; (from 88 kHz & 112 kHz)

Stopband = 140kHz, -35dB (approximately at 30kHz & 170kHz);

Gain = 1;

Type: 6^{th} order Chebychev with 0.1dB ripple

BASEBAND LPF

$F_{cut\text{-}off}$ = 1.6 kHz;

Gain = 0.9;

Type: 4^{th} order Butterworth

Divider:

Digital Logic Level Input & Output Signals 0 to 5V

Division Factors -1, /2, /4, /8 (switch selectable by user)

Bandwidth approx. 1MHz

Dual Analog Switch & Sample/Hold:

Analog Input Bandwidth 50kHz

Maximum CONTROL clock 100kHz

CONTROL Input Levels digital-level only, 0V and 5V

Maximum Analog Input Level 4Vpk-pk

Exclusive-OR:

Dual Logic Level Input

Output is Logical Exclusive-OR Function.

Expansion:

EXPANSION module allows optional modules to be installed and used with the ETT-101

Headphone Amplifier:

Output power 125mW, stereo socket

Headphone Type and Connector 3.5mm stereo, > 8ohm impedance

Line Code Encoder:

Input data from SEQUENCE GENERATOR "X" data sequence

CLK same digital-level clock as SEQUENCE GENERATOR CLK signal,

fmax > 100kHz

Line codes: NRZ-L, RZ-AMI, Bi-phase, NRZ-M

Output LINE-CODE signal +/-2Vp-p

Master Signals:

Output Frequencies carrier: 100kHz in quadrature and a third digital signal

sample clock 8.333kHz (sub-multiple of the carrier)

message: 2.083kHz sinusoidal and digital,

Output Levels 4V pk-pk, analog (+/- 5%)

Digital level, 0V to 5V

Multipliers:

3 independent dual input multipliers

Bandwidth approx 600kHz

Characteristic k.X(t).Y(t)

k approx 1

Noise Generator:

Bandwidth 10Hz to < 240kHz, "white" noise

Maximum level approx 4.8Vrms

Attenuator steps 0dB (approx 4.8Vrms), -6dB (approx 2.4Vrms) and -20dB (approx 0.48Vrms)

PCM Encoder:

Input Vin +/-2Vpk, DC coupled

Bit Clock Input >128kHz, digital-level

Output Signal serial, digital-level data stream in offset binary format

Output Format 8 bits data

Frame Synchronization FS synchronization signal coincident with frame's LSB

TDM Mode two input Time Division Multiplex system

No anti-aliasing filters

PCM Decoder:

Input PCM DATA serial, digital-level data stream in offset binary format

Input Format 8 bits

Bit Clock Input <128kHz, digital-level;

Output Signal approximately +/-2Vpk, DC coupled

TDM Mode two channel TDM system

Outputs do not include reconstruction filters

Phase Shifter:

Bandwidth > 200kHz

Frequency Ranges two regions

HI approx 100kHz;

LO approx 2kHz

Auto detect HI/LO boundary approx. 40kHz

Sequence Generator:

Input Clock Range TTL 1Hz to 100kHz

Number of Sequences 2: X and Y

Sequence Lengths X = 31 bits, Y = 255 bits

Sync indicates start of sequence X

Serial to Parallel:

Inputs SERIAL digital-level data;

CLK is the digital-level clock signal;

Maximum CLK Rate approx 100kHz

Outputs bipolar parallel data output

Speech:

Microphone electret-type with frequency response of 300Hz to 3kHz

Output typically 0.6 Vrms

Tuneable LPF:

Filter Range 600 Hz to 12 kHz

Filter Order 8th order, Elliptic

Stopband Attenuation > -50dB at 1.4 f_c and Passband Ripple < 0.5dB

Gain Control 0 to 1.6

Twin Pulse Generator:

Clock Frequency Range < 8kHz

Pulse WIDTH 5us < t_w < 40us

Pulse DELAY Q2-Q1 50us < t_d < 300us

Utilities:

COMPARATOR

Operating Range > 100kHz

TTL Output Risetime 500nsec (typically)

RECTIFIER

Bandwidth DC to 100kHz (approx)

DIODE & LPF

LPF -3dB 2.6kHz (approx)

RC LPF

LPF -3dB 2.6kHz (approx)

Variable DC V:

DC V Terminal +/-2.5V, <5mA

+5V DC Terminal +5V, <10mA

VCO:

Frequency Ranges

1kHz < LO < 17kHz; sinewave and digital-level

60kHz < HI < 140kHz; sinewave and digital-level

Input Voltage -3V < VCO INPUT < 3V

GAIN G.Vin : 1 < G < 2

SYSTEM SPECIFICATIONS

STANDARD ACCESSORIES

Patch Cords 20 x 2mm-2mm stackable patch cords

Scope leads 3 x 2mm-to-BNC coaxial oscilloscope leads

Headphones 1 x lightweight stereo headphones, 24ohm, 3.5mm male, stereo

Plug Pack multi-input voltage with 12V/1A output, regulated. Tip is positive;

Multiple input voltage, multiple international certifications.

Documentation 1 x User Manual; 2 x Experiment Manuals (Vol.1 and Vol.2)

POWER SUPPLY

Power Source multi-voltage plug pack supplied as standard
Power Supply 12V to 15V DC, 1A maximum

Protection reverse polarity and self-resetting circuit breaker protection above 16V input.

Absolute Maximum Supply Input 30V DC

ENVIRONMENTAL

Operating Temperature Range 10 to 30 degrees C

Storage Temperature Range 5 to 40 degrees C

Humidity up to 90% RH, non-condensing

PHYSICAL

Case Dimensions front panel 280 x 232mm; height 32 to 70mm

The following conventions shall be used.

- Each Plug-in module shall be a functional electronic circuit, utilized in numerous experiments.
- A Master Signals module shall provide synchronized 100kHz Sine and Cos outputs for use as carrier signal, (approx.) 100kHz, 8kHz, and 2kHz digital outputs and a 2kHz sine.
- 2 mm Sockets shall be provided on the front panel to facilitate patching of the modules.
- For each defined module, sockets on the Left Hand Side shall be signal Inputs and sockets on the Right Hand Side are for signal Outputs.
- Input and Output impedances shall be intentionally mismatched, so that the signal connections may be made of broken without changing signal amplitudes at module outputs.
- Sockets carrying digital signals shall be identified with a “square” surround and analog signals and common signals with a “round” surround.
- No signal can be generated that can cause any self-damage to the unit in any way.
- Inputs and outputs shorted together or joined together, shall not cause any damage to the unit.
- Patching of modules shall be carried out at any time during an experiment without any risk of causing damage to unit.
- All modules shall be labelled so as to identify the basic electronic circuit function performed.
- Variable controls shall not have calibration marks so that the user achieves correct experiment implementation by observing and adjusting signals.

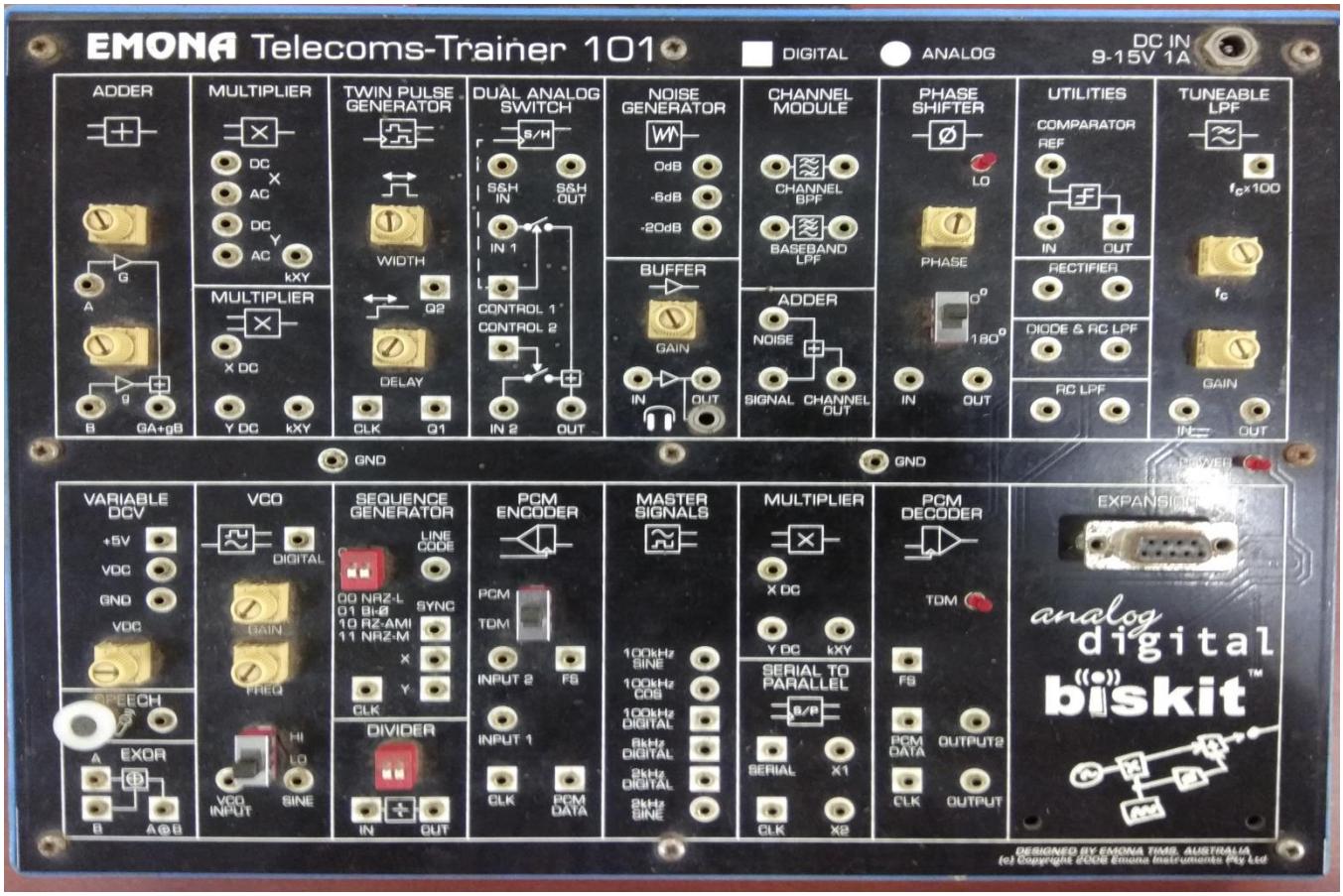
Detailed Experiment Requirements

Basic Experiment Topics covered:

1. Setting up an Oscilloscope
2. An Introduction to the Experimenter
3. Modelling Equations
4. Amplitude Modulation AM
5. Double Sideband DSB Mod
6. AM Demodulation
7. DSB Demodulation
8. SSB Modulation and Demodulation
9. FM Modulation
10. FM Demodulation
11. Sampling & Reconstruction
12. PCM Encoding
13. PCM Decoding
14. BW Limiting and Restoring Digital Signals
15. ASK Modulation and Demodulation
16. FSK Modulation and Demodulation
17. BPSK Modulation and Demodulation
18. QPSK Modulation and Demodulation
19. Intro to Spread Spectrum - DSSS Mod.
20. Introduction to Undersampling in SDR

Advanced Experiment Topics covered:

1 - AM (method 2) & product detection
2 - Noise in AM communications
3 - PCM & time division multiplexing (TDM)
4 - An intro to Armstrong's modulator
5 - Phase division modulation and demod
6 - Pulse-width modulation & demodulation
7 - Message translation & inversion
8 - Carrier acquisition using the PLL
9 - SNR & eye diagrams
10 - PCM and SNDR
11 - ASK demod using product detection
12 - FSK generation (switching method) & demod.
13 - Principles of GFSK
14 - PN sequence spectra and noise generation
15 - Line coding and bit clock regeneration
16 - Delta modulation & demodulation
17 - Delta-sigma modulation & demodulation
18 - Observations of AM & DSBSC signals in the freq domain
19 – Demonstrating the principles of superheterodyne
20 – Frequency synthesis using a digital PLL
21 – Differential phase shift keying (DPSK)
22 – PAM and time division multiplexing (TDM)


EMONA Telecoms-Trainer 101
DIGITAL
ANALOG
DC IN
9-15V 1A
ADDER
MULTIPLIER
TWIN PULSE GENERATOR
DUAL ANALOG SWITCH
NOISE GENERATOR
CHANNEL MODULE
PHASE SHIFTER
UTILITIES
TUNEABLE LPF
MULTIPLIER
BUFFER
ADDER
GND
GND
POWER
VARIABLE DCV
VCO
SEQUENCE GENERATOR
PCM ENCODER
MASTER SIGNALS
MULTIPLIER
PCM DECODER
EXPANSION
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